AMENDMENTS TO THE CLAIMS

Claim 1 (original): A semiconductor memory device, comprising:

a memory cell array comprising a two-value memory region and a multi-value memory region, wherein the two-value memory region comprises a plurality of memory cells each storing 1-bit data and the multi-value memory region comprises a plurality of memory cells each storing 2 or more-bit data; and

a sense amplifier section common to data read of the two-value memory region and data read of the multi-value memory region, for reading data stored in a selected memory cell by comparing a potential of the selected memory cell with a reference potential.

Claim 2 (original): A semiconductor memory device according to claim 1, further comprising:

a first switch section for switching the reference potential, depending on whether data is read from the two-value memory region or the multi-value memory region.

Claim 3 (original): A semiconductor memory device according to claim 1, further comprising:

a conversion section for changing the number of bits in accordance with a result of a comparison performed by the sense amplifier section, and switching output data, depending on whether or not the data is read from the multi-value memory region or the two-value memory region.

Claim 4 (original): A semiconductor memory device according to claim 3, wherein:

the conversion section has two or more output terminals; and

when data is read from the two-value memory region, the conversion section outputs the data through the output terminals, all bits of the data having the same value.

Claim 5 (original): A semiconductor memory device according to claim 1, further comprising:

a redundant cell for replacing a defective memory cell in the memory cell array, if any; and

a switch section for receiving data read from the selected memory cell and data read from the redundant cell, and switching from the data read from the selected memory cell to the data read from the redundant cell when the selected memory cell is the defective memory cell.

Claim 6 (original): A semiconductor memory device according to claim 1, further comprising:

a write/delete control section for controlling data write or data delete for the two-value memory region and the multi-value memory region separately,

wherein the sense amplifier section can perform data read for one of the two-value memory region and the multi-value memory region while the write/delete control section is performing data write or data delete for the other of the two-value memory region and the multi-value memory region.

Claim 7 (original): A semiconductor memory device according to claim 1, further comprising:

a write/delete control section for controlling data write or data delete for the two-value memory region and the multi-value memory region separately,

wherein the write/delete control section can perform data write or data delete for one of the two-value memory region and the multi-value memory region while the sense amplifier section is

performing data read for the other of the two-value memory region and the multi-value memory region.